Syllabus: Introduction to Flip-Flops, NAND Gate Latch/ NOR Gate Latch, RS Flip-Flop, Gated Flip-Flops : Clocked RS Flip-Flop.

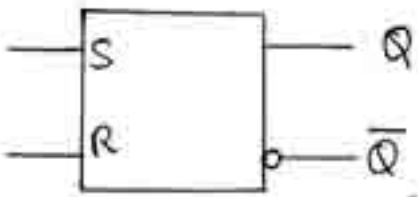
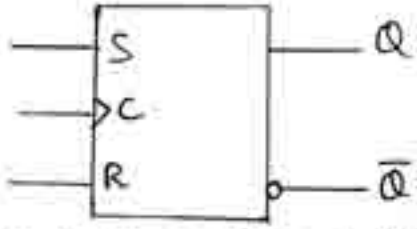
* Introduction:

Latch: Latch is a bistable element, whose output changes when its input change.

Flip-Flop: Flip-Flop is a bistable element, whose output changes only either at the rising (or) falling edge of the enable signal (clock signal)

Note:

① Comparision of Latch & Flip-Flop:

Latch	Flip-Flop (Bistable multivibrator)
① Latch is a bistable element, whose output changes when its input changes (Sometime clock signal may be present)	① Flip-Flop is a bistable element, whose output changes only either at the rising (or) falling edge of the enable signal (clock signal)
② It doesnot require any external timing signals (Asynchronous device)	② It require special timing signal called the clock (Synchronous device)
③ Output changes when its input changes	③ Its content (output) remains constant even if the input changes
④ Symbol of Latch is shown in fig①  Active high input S-R Latch (Fig①)	④ Symbol of Flip-Flop is shown in fig②  Positive edge triggered SR FF (Fig②)

⑤ The input lines are continuously being interrogated	⑤ Inputs are normally sampled & not interrogated continuously.
⑥ It is the basic element for storing information (can store one bit of information)	⑥ It is the basic element for storing information (can store one bit of information)

② IEEE Logic Symbols & Traditional Logic-gate Symbols

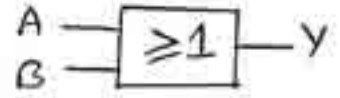
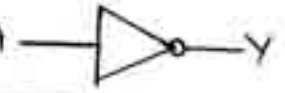
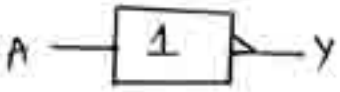
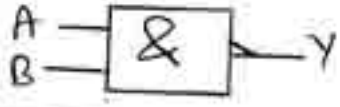
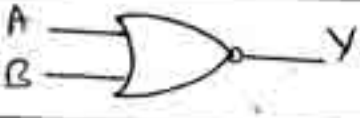
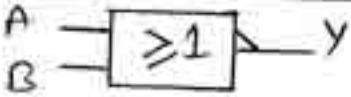
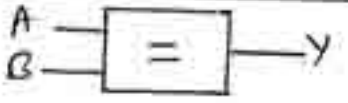
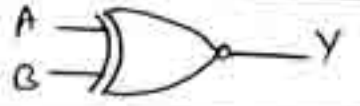
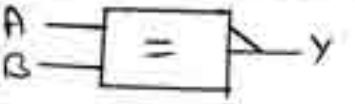
Logic function	Traditional Logic Symbol	IEEE Logic Symbol
AND		
OR		
NOT		
NAND		
NOR		
XOR		
XNOR		

Table ③

③ Two Categories of Flip-Flops:

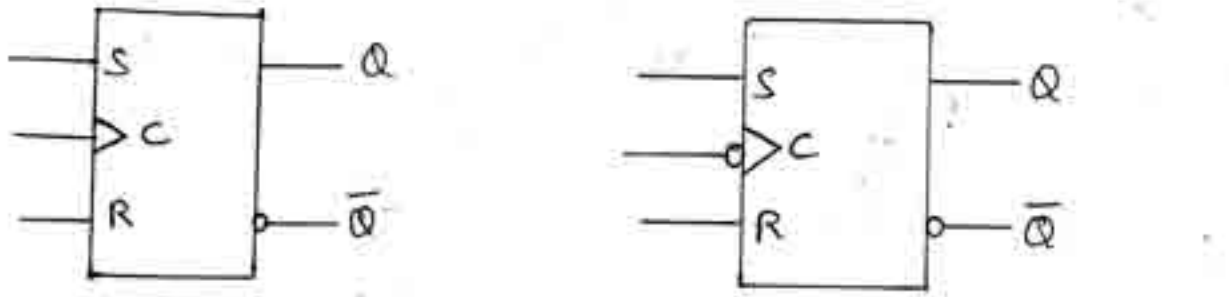
ⓐ Edge-Triggered Flip-Flops

The term edge-triggered means that the flip-flop changes state either at the positive edge (rising edge)

(or) at the negative edge (falling edge) of the clock pulse & is sensitive to its inputs only at this transition of the clock.

Three basic types of edge-triggered flip-flops:
(i) S-R (ii) D & (iii) J-K.

The logic symbol is shown in fig(4)



(a) Positive edge-triggered (b) negative edge-triggered

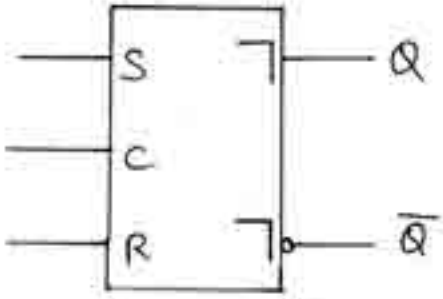
Fig(4): Edge-triggered flip-flop

(b) Pulse-Triggered (Master-Slave) Flip-Flops

The term pulse-triggered means that data are entered into the flip-flop on the leading edge of the clock pulse, but the output doesnot reflect the input state until the trailing edge of the clock pulse. The inputs must be setup prior to the clock pulse's leading edge, but the output is postponed until the trailing edge of the clock.

Three basic types of pulse-triggered flip-flops:
(i) S-R (ii) D & (iii) J-K.

The logic symbol is shown in fig(5)



Fig(5): Pulse-triggered (master slave) flip-flop

* SR Latch @ RS Latch

The simplest type of Latch is SR Latch. It has 2 inputs, namely SET (S) & RESET (R), and 2 outputs Q and $\bar{Q}$.

The SR Latch can be implemented using NAND gates @ NOR gates

(a) NAND Gate Latch @ SR Latch using NAND gates @ RS Latch using NAND gates :

The NAND gate based SR Latch is shown in fig (6)(a) It consists of cross connected NAND gates.

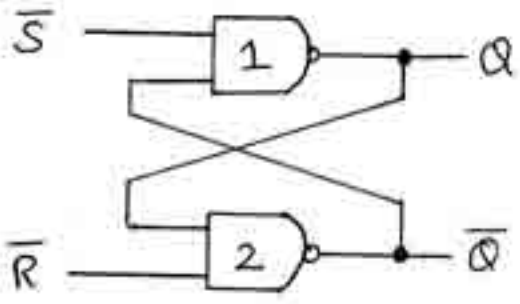


Fig 6(a) : Circuit diagram

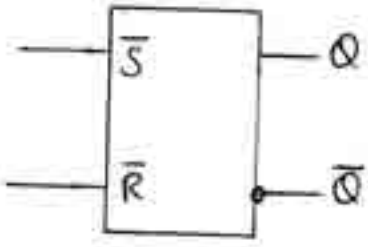


Fig 6(b)

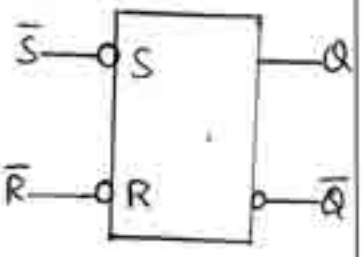


Fig 6(c)

The logic Symbol of SR Latch is shown in fig 6(b).
The IEEE Symbol of SR Latch is shown in fig 6(c).

Operation :

Case 1: $\bar{S}=1, \bar{R}=1$

(a) Let $Q=1$ ($\bar{Q}=0$): The inputs to the gate 1 are $\bar{S}=1$ & $\bar{Q}=0$, So its output is $Q=1$ (No change)
The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$ (No change)

(b) Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $\bar{S}=1$ & $\bar{Q}=1$, So its output is $Q=0$ (No change)
The inputs to the gate 2 are $\bar{R}=1$ & $Q=0$. So its

output is $\bar{Q}=1$ (No change)

∴ When $\bar{R}=1$, $\bar{S}=1$, the output remains in the previous state (Last state) or output doesnot change.

Case 2: $\bar{S}=0$, $\bar{R}=1$

ⓐ Let $Q=1$ ($\bar{Q}=0$): The inputs to the gate 1 are $\bar{S}=0$ & $\bar{Q}=0$, So its output is $Q=1$.

The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$.

ⓑ Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $\bar{S}=0$ & $\bar{Q}=1$, So its output is $Q=1$.

The inputs to the gate 2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$

or

The input to gate 1 is $\bar{S}=0$, So its output is $Q=1$. Now inputs to the gate-2 are $\bar{R}=1$ & $Q=1$, So its output is $\bar{Q}=0$.

∴ When $\bar{S}=0$, $\bar{R}=1$, the output is Set ($Q=1$)

Case 3: $\bar{S}=1$, $\bar{R}=0$

The input to gate 2 is $\bar{R}=0$, So its output is $\bar{Q}=1$. Now inputs to the gate-1 are $\bar{S}=1$ & $\bar{Q}=1$, So its output is $Q=0$.

∴ When $\bar{S}=1$, $\bar{R}=0$, the output is Reset ($Q=0$)

Case 4: $\bar{S}=0$, $\bar{R}=0$

When $\bar{S}=0$, $\bar{R}=0$, both the outputs Q & $\bar{Q}$ try to become 1, which is not possible.

The Condition $\bar{S}=\bar{R}=0$ is avoided because it results in an invalid mode of operation (Forbidden state) [Major drawback

of any SET-RESET type of Latch]

The truth table of NAND gate Latch is shown in fig 6(d)

Inputs		outputs		Comments
$\bar{S}$	$\bar{R}$	Q	$\bar{Q}$	
1	1	NC	NC	No change. Latch remains in previous state
0	1	1	0	LAtch SETS
1	0	0	1	Latch RESETS
0	0	1	1	Invalid condition

Fig 6(d)

(b) NOR Gate Latch (a) SR Latch using NOR gates (or) RS Latch using NOR gates :

The NOR gate based SR Latch is shown in fig 7(a)

It consists of cross connected NOR gates.

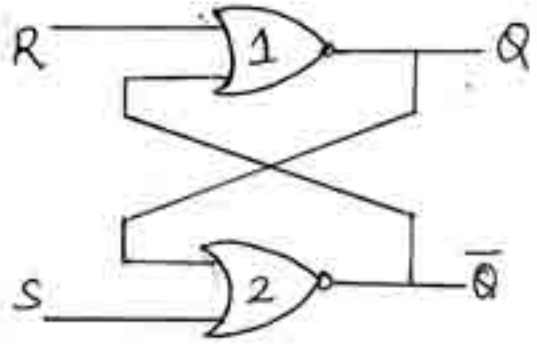


Fig 7(a): circuit diagram

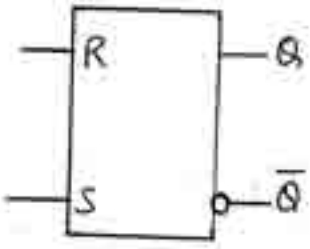


Fig 7(b)

The logic Symbol of SR Latch is shown in fig 7(b)

Operation;

Case 1: R=0, S=0

(a) Let Q=1 ($\bar{Q}$=0): The inputs to the gate 1 are R=0 & $\bar{Q}$=0, So its output is Q=1 (No change)

The inputs to the gate 2 are S=0 & Q=1, So its output

is $\bar{Q}=0$ (No change)

(b) Let $Q=0$ ($\bar{Q}=1$): The inputs to the gate 1 are $R=0$ & $\bar{Q}=1$, So its output is $Q=0$ (No change)

The inputs to the gate 2 are $S=0$ & $Q=0$, So its output is $\bar{Q}=1$ (No change)

∴ When $R=S=0$, the output remains in the previous state.

Case 2: $R=0, S=1$

The input to gate 2 is $S=1$, So its output is $\bar{Q}=0$. Now inputs to gate 1 are $R=0$ & $\bar{Q}=0$. So its output is $Q=1$.

∴ When $R=0, S=1$, the output is Set ($Q=1$)

Case 3: $R=1, S=0$

The input to gate 1 is $R=1$, So its output is $Q=0$. Now inputs to gate 2 are $S=0$ & $Q=0$. So its output is $\bar{Q}=1$.

∴ When $R=1, S=0$, the output is Reset ($Q=0$)

Case 4: $R=1, S=1$

When $R=S=1$, both the outputs Q & $\bar{Q}$ try to become 0, which is not possible.

The condition $R=S=1$, is avoided because it results in an invalid mode of operation (Forbidden State).

The truth table of NOR gate Latch is shown in fig 7©

Inputs		outputs		Comments
R	S	Q	$\bar{Q}$	
0	0	NC	NC	No change. Latch remains in Previous state
0	1	1	0	Latch SETS
1	0	0	1	Latch RESETS
1	1	0	0	Invalid condition

Fig 7©

Note:

① The outputs $Q/\bar{Q}$ can also be denoted by $X/\bar{X}$ @ $A/\bar{A}$

② Q is Normal FF output, $\bar{Q}$ is inverted FF output.

③ $Q=1, \bar{Q}=0$ → SET State @ 1 State @ High State.

④ $Q=0, \bar{Q}=1$ → LOW State @ 0 State @ CLEAR @ RESET State

⑤ In NAND gate SR Latch, instead of $\bar{S}$ & $\bar{R}$ (inputs), S & R can be used. 111^{th} in NOR gate SR Latch. instead of S & R, $\bar{S}$ & $\bar{R}$ can be used.

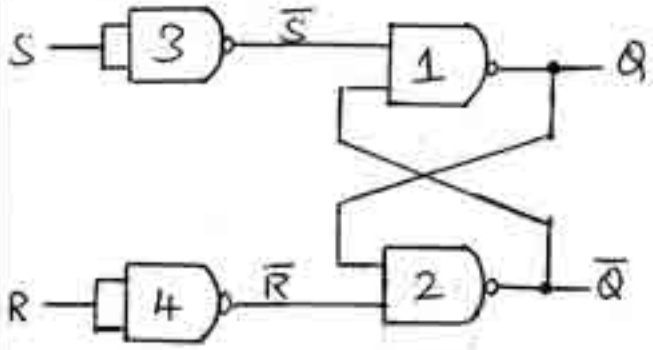
⑥ Sometimes NAND gate based SR Latch is called as $\bar{S}\bar{R}$ Latch (because inputs are $\bar{S}$ & $\bar{R}$)

⑦ RS Flip-Flop (or) RS Flip-flop Latch @ NAND Gate SR Latch

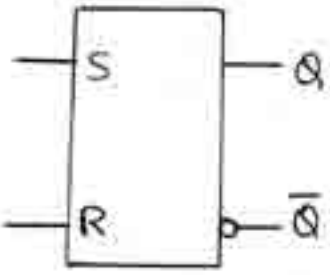
Fig ⑧ shows RS Flip-flop (alternative way of NAND Gate SR Latch implementation)

Explanation is same as NAND Gate SR Latch (page 4)

Case 1: $\bar{S}=1, \bar{R}=1$ ($\Leftrightarrow S=0, R=0$)



(a) Circuit diagram of RS flip-flop latch



(b) Logic Symbol

Inputs		Outputs		Comments
S	R	Q	$\bar{Q}$	
0	0	NC	NC	Last State (or) No change (or) Previous State
1	0	1	0	SET
0	1	0	1	RESET
1	1	1	1	Invalid condition (forbidden)

(c) Truth table

Fig(8) : RS-FLIP-flop

Case 2: $\bar{S}=0$, $\bar{R}=1$ ($\Rightarrow S=1, R=0$)

Case 3: $\bar{S}=1$, $\bar{R}=0$ ($\Rightarrow S=0, R=1$)

Case 4: $\bar{S}=0$; $\bar{R}=0$ ($\Rightarrow S=1, R=1$)

Gates (3) & (4) can be replaced by NOT gates (or) NOR gates.

Gated Flip-flops (Clocked RS Flip-flops) (Enable RS FFs)

Clocked RS Flip-flop using NAND gates

The Clocked RS NAND gate flip-flop is shown in fig (a)

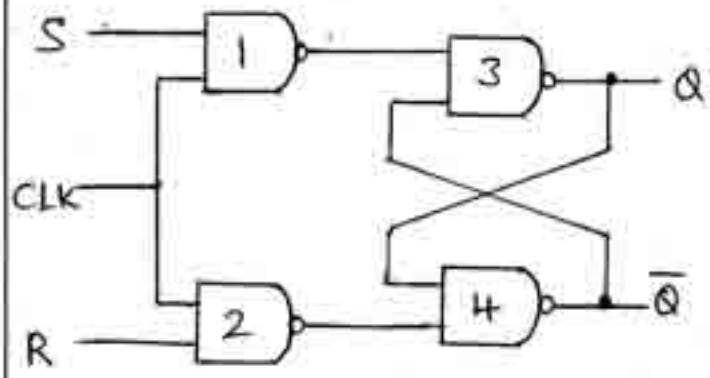


Fig (a): circuit diagram

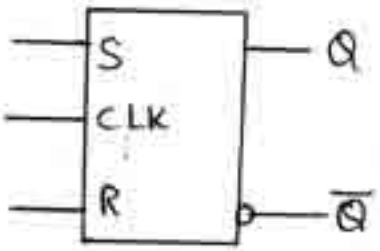


Fig (b): Logic Symbol

The logic Symbol of clocked RS NAND gate flip-flop is shown in fig (b).

Operation:

- **Clock is Low (CLK = 0):**

When the clock is low, the output of gates 1 and 2 is high(1). Hence the output of gates 3 & 4 will not change regardless of S & R input values.

∴ When CLK = 0, S = X, R = X, the output remains in the previous state.

- **Clock is high (CLK = 1):**

Case 1: S = 0, R = 0

When R = S = 0, the output remains in the previous state. (CLK = 1)

Case 2: S = 1, R = 0

When S = 1, R = 0 & CLK = 1, the output is Set (Q = 1)

Case 3: S = 0, R = 1

When S = 0, R = 1 & CLK = 1, the output is Reset (Q = 0)

Case 4: S = 1, R = 1

When S = R = CLK = 1, both the outputs Q & $\bar{Q}$ try to

become 1, which is not possible (Invalid condition @ Forbidden state)

The truth table of clocked RS NAND gate flip-flop is shown in fig 9©.

Inputs			outputs		Comments
CLK	S	R	Q	$\overline{Q}$	
0	X	X	NC	NC	No change (previous State)
1	0	0	NC	NC	No Change (Previous State)
1	1	0	1	0	SET
1	0	1	0	1	RESET
1	1	1	1	1	Invalid

Fig 9© : Truth table of clocked RS NAND gate FF

b) Clocked RS Flip-flop using NOR gates

The clocked RS NOR gate flip-flop is shown in fig 10@

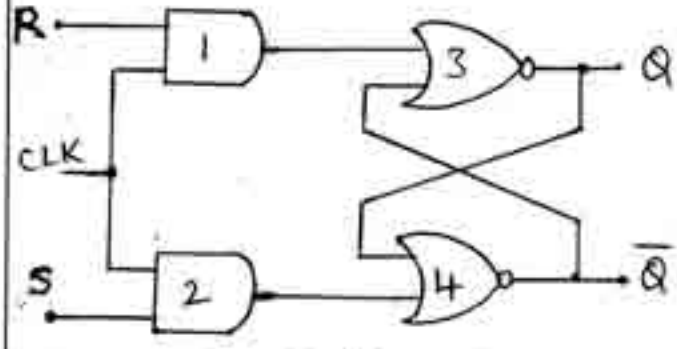


Fig 10@ : Circuit diagram

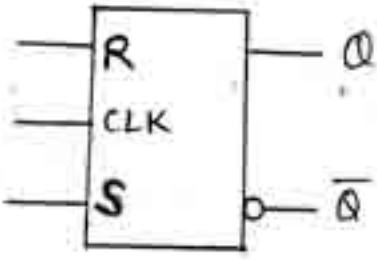


Fig 10ⓑ: Logic Symbol

The logic Symbol of clocked RS NOR gate flip-flop is shown in fig 10ⓑ.

Operation:

- Clock is Low (CLK=0):

When the clock is low, the output of gates 1 and 2 is Low(0). Hence the output of gates 3 & 4 will not change regardless of S & R input values.

∴ When CLK = 0, S = X, R = X, the output remains in the previous state.

- Clock is high (CLK = 1):

Case 1: R = 0, S = 0

When R = S = 0 & CLK = 1, the output remains in the previous state.

Case 2: R = 0, S = 1

When R = 0, S = 1 & CLK = 1, the output is Set (Q = 1)

Case 3: R = 1, S = 0

When R = 1, S = 0 & CLK = 1, the output is Reset (Q = 0)

Case 4: R = 1, S = 1

When R = S = CLK = 1, both the outputs Q & $\bar{Q}$ try to become 0. Which is not possible (Invalid Condition & Forbidden state)

The truth table of Clocked RS NOR gate flip-flop is shown in fig 10©

Inputs			Outputs		Comments
CLK	R	S	Q	$\bar{Q}$	
0	X	X	NC	NC	No Change (Previous State)
1	0	0	NC	NC	No Change (Previous State)
1	0	1	1	0	SET
1	1	0	0	1	RESET
1	1	1	0	0	Invalid Condition

Fig 10© : Truth table of Clocked RS NOR gate FF

Note: X → Don't care (1 or 0)

Problems

① If the $\bar{S}$ & $\bar{R}$ waveforms in fig 1@ are applied to the inputs of the Latch of fig 1⑥, determine the waveform that would be observed on the Q output. Assume that Q is initially Low.

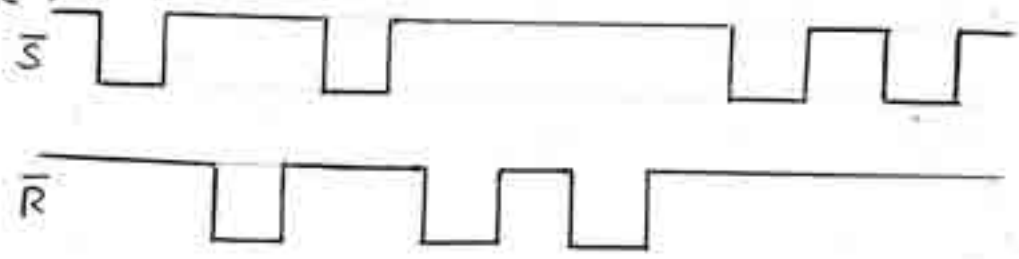


Fig 1@

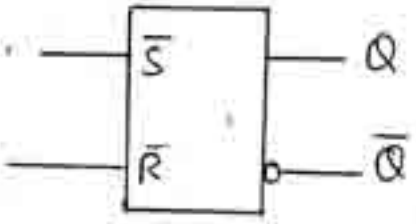
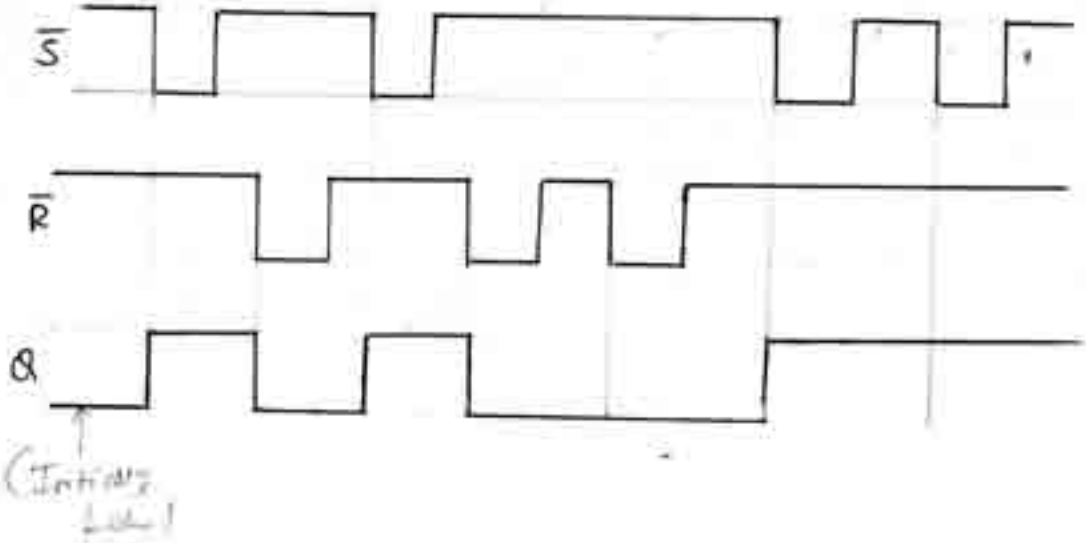


Fig 1⑥

Sol: We have truth table of SR Latch

Inputs		o/p
$\bar{S}$	$\bar{R}$	Q
1	1	NC
0	1	1
1	0	0
0	0	1



② Construct the TT for the circuit shown in fig ②

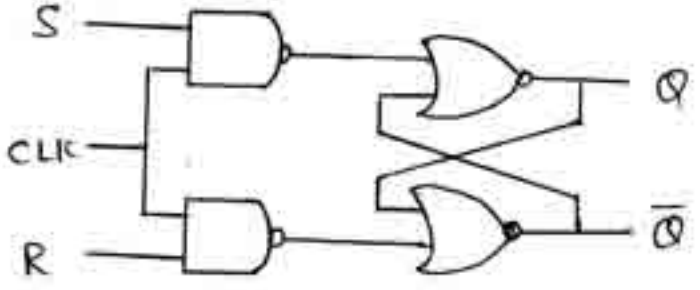
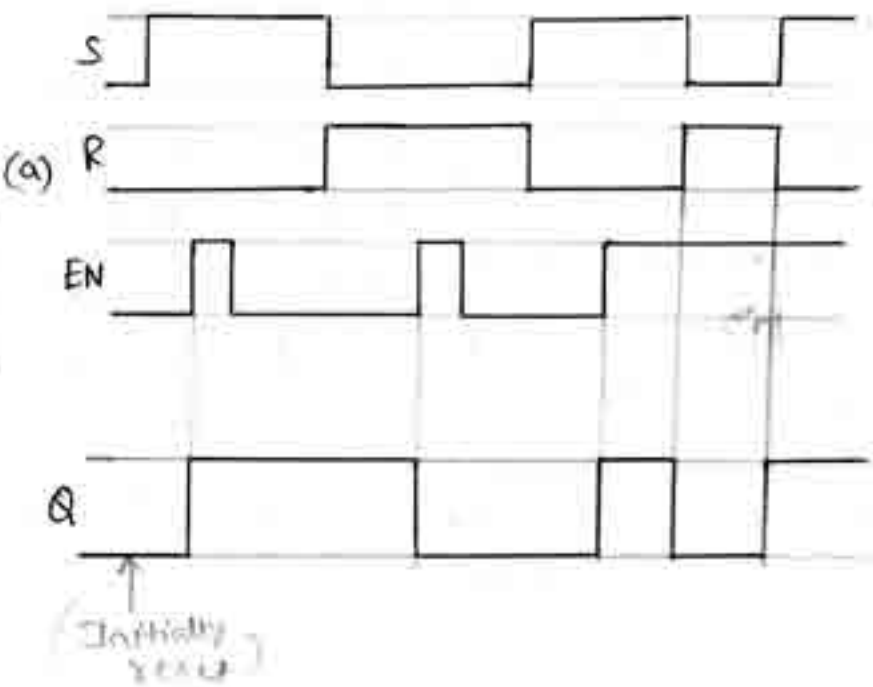


Fig ②

Sol: Inputs outputs

CLK	S	R	Q	$\bar{Q}$	
0	X	X	0	0	Invalid
1	0	0	0	0	
1	0	1	0	1	→ Reset
1	1	0	1	0	→ Set
1	1	1	NC	NC	Previous State

3) Determine the Q-output waveform if the inputs shown in fig 3(a) are applied to a gated S-R Latch that is initially RESET



(a)

d:

Inputs			output
CLK	S	R	Q
0	X	X	Q(NC)
1	0	0	Q (NC)
1	1	0	1
1	0	1	0
1	1	1	Invalid (Avoided)