BT-4/M-12 **8406**

DIGITAL ELECTRONICS

Paper-ECE-204E

Time Allowed: 3 Hours] [Maximum Marks: 100

Note: Attempt **five** questions in all, selecting at least **one** question from each Section.

SECTION-I

1. (a) Differentiate between :
(i) Digital Signal and Analog Signal
(ii) XOR gate and XNOR gate. 6

(b) Convert $(0.65625)_{10}$ to binary. 4

(c) What are the important characteristics of Gray code? 4

(d) Express the following BCD numbers in
(i) Straight binary form and (ii) Excess-3 code.
10010011, 01100111. 6

2. (a) Realize or implement the following Boolean expression using basic gates:
$Y = \overline{AC} + \overline{BC} + BC + AC$ 6

(b) Minimize the following Logic function and realize using NOR gates:
F (A, B, C, D) = πM (1, 2, 3, 8, 9, 10, 11, 14) . d (7, 15). 8

(c) How is QM method of simplification different from K-map method? 6

SECTION-II

3. (a) Realize full subtractor using NAND gates only, if *I/P's* A, B and b_i are available in complemented. 6

(b) Implement the following Boolean function using 8 : 1 multiplexer :
F (A, B, C, D) = ∑m (O, 2, 6, 10, 11, 12, 13) + ∑d (3, 8, 14) 8

(c) Draw common anode and common cathode circuits of LED seven segment display and bring out the difference between them. 6

4. (a) Draw and explain working of a positive edge triggered J-K flip flop.
Also explain the race around problem. 7

(b) Discuss the application of Shift registers. 5

(c) Design a synchronous counter with the following sequence:
0001 → 0011 → 0101 → 0111 → 1001 → 1011 → 1101 → 1111 → 0001……. 8

SECTION-III

5. (a) Discuss the switching mode operation of p-n junction. 7

(b) Explain the parameters used to characterize logic families. 7

(c) How fan out is increased in DTL? Justify your answer. 6

6. (a) What is interfacing? What are the different schemes for CMOS and TTL interface? Explain one of them. 10

(b) Compare CMOS and TTL families. 5

(c) What are the applications of open collector output? 5

SECTION-IV

7. (a) What are the disadvantages of weighted register DAC? 6

(b) Explain the important specifications of DAC. 6

(c) An 8 bit ADC accepts an input voltage 0 to 10 V
(i) What I/P voltage will cause all l's at the ADC output?
(ii) What is the digital output code, if the applied I/P voltage is 5.2V? 8

8. (a) What is meant by the term 'architecture of PLD' ? Give some suitable examples. 8

(b) Discuss the applications of PLAs. 5

(c) What is programmable array logic? How does it differ from ROM? 7