

Roll No.

Total No. of Pages : 3

BT4/M06

8764

Digital Electronics (New)

Paper : ECE-204 E

Time : Three Hours]

[Maximum Marks : 100

Note :- Attempt **FIVE** questions selecting at least **ONE** question from each part. Each question carries equal marks.

PART-I

1. Perform the indicated operation :-

(i) Express the decimal number (-46) as an 8-bit binary number in the 2's complement form.

(ii) Add the signed numbers :-

$01000100, 00011011, 00001110$ and 00010010 .

(iii) Subtract the signed numbers :-

$-120 - (-30)$.

(iv) Convert into decimal :- $B2F8_{16}$.

(v) Encode $(11000110)_2$ to Gray code.

(vi) Convert Gray code (100111) to binary.

(vii) Encode $(327.89)_{10}$ to excess-3 code.

(viii) Design 'AND' 'OR' gates using NOR gates only.

(ix) Convert $(1100111001.0001011110011)_2$ into octal equivalent.

(x) Find the decimal equivalent of the following binary numbers assuming sign magnitude representation :-

(a) 1011100

(b) 010100 .

$10 \times 2 = 20$

2. (a) Using the K-map minimize the function in the SOP form and implement the circuit using NAND gates only :- 15
 $F(A, B, C, D) = \sum m(2, 3, 8, 10, 11, 12, 14, 15)$
 (b) Write a short note on universal property of NAND, NOR gates. 5

PART-II

3. (a) BCD numbers are applied sequentially to the BCD to decimal decoder (having active high inputs and active low outputs). Draw the ten output waveforms, showing each in the proper relationship to the others and to the inputs. 15

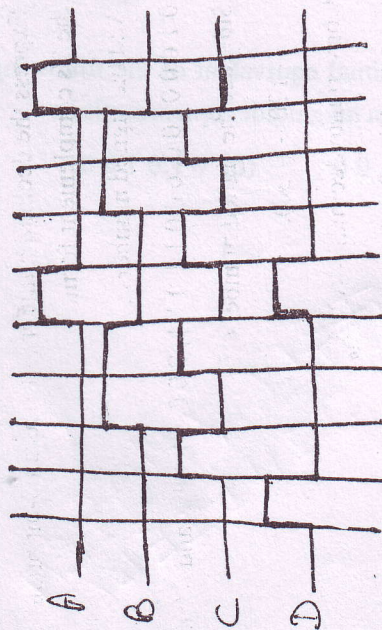


Fig : BCD numbers for Q. No. 3(a)

- (b) Design a BCD adder circuit and discuss its operation. 5
 4. (a) What is non critical race around condition ? Discuss the methods for avoiding this problem. 5
 (b) Develop a Synchronous three bit up/down counter with a Gray code sequence. The counter should count up when up/down control input is '1' and count down when the control input is '0'. 15

PART-III

5. Describe the operation of a TTL circuit. What are the TD TEM pole and open collector outputs ? Discuss with their circuit diagrams. Use open collector inverters to implement the following logic expressions :-

(a) $X = \bar{A} \bar{B} \bar{C}$ (b) $X = A \bar{B} C \bar{D}$ (c) $X = A B C \bar{D} \bar{E} \bar{F}$. 20

6. (a) Obtain the change in the fan out and noise margins if in the circuit of DTL :-
 (a) One of the series diode is removed.
 (b) One more diode is inserted in series (total 3 diodes in series). 10

- (b) What is CMOS ? Draw and discuss the NAND, NOR gates using CMOS logic family. Compare the performance of CMOS & TTL. 10

PART-IV

7. (a) Draw the block diagram and flowchart of successive approximation ADC and illustrate the operation of 4-bit SAC using DAC step size '1V' and analog input $V_A = 10.4V$. 15
 (b) Find out the output voltage from a six bit binary ladder with following digital inputs (i) 1 0 1 0 0 1 (ii) 1 1 0 0 0 1
 Assume the input levels as '0' = 0V and '1' = +10V. 5

8. Write a short note on each of the following :-

- (a) ROM
 (b) PLA
 (c) FPGA
 (d) CPLD. 20